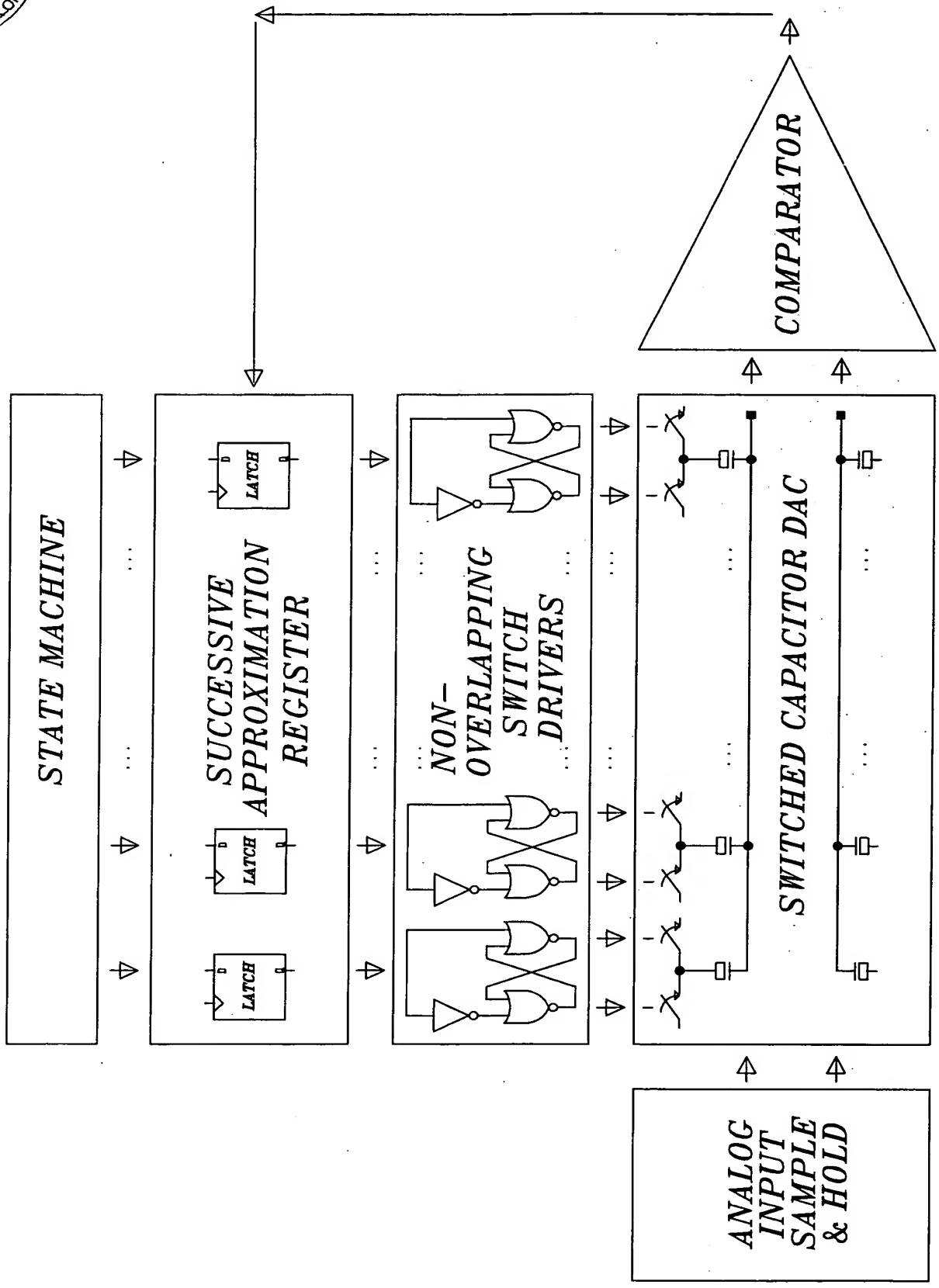

FIG. 1 (Prior Art)

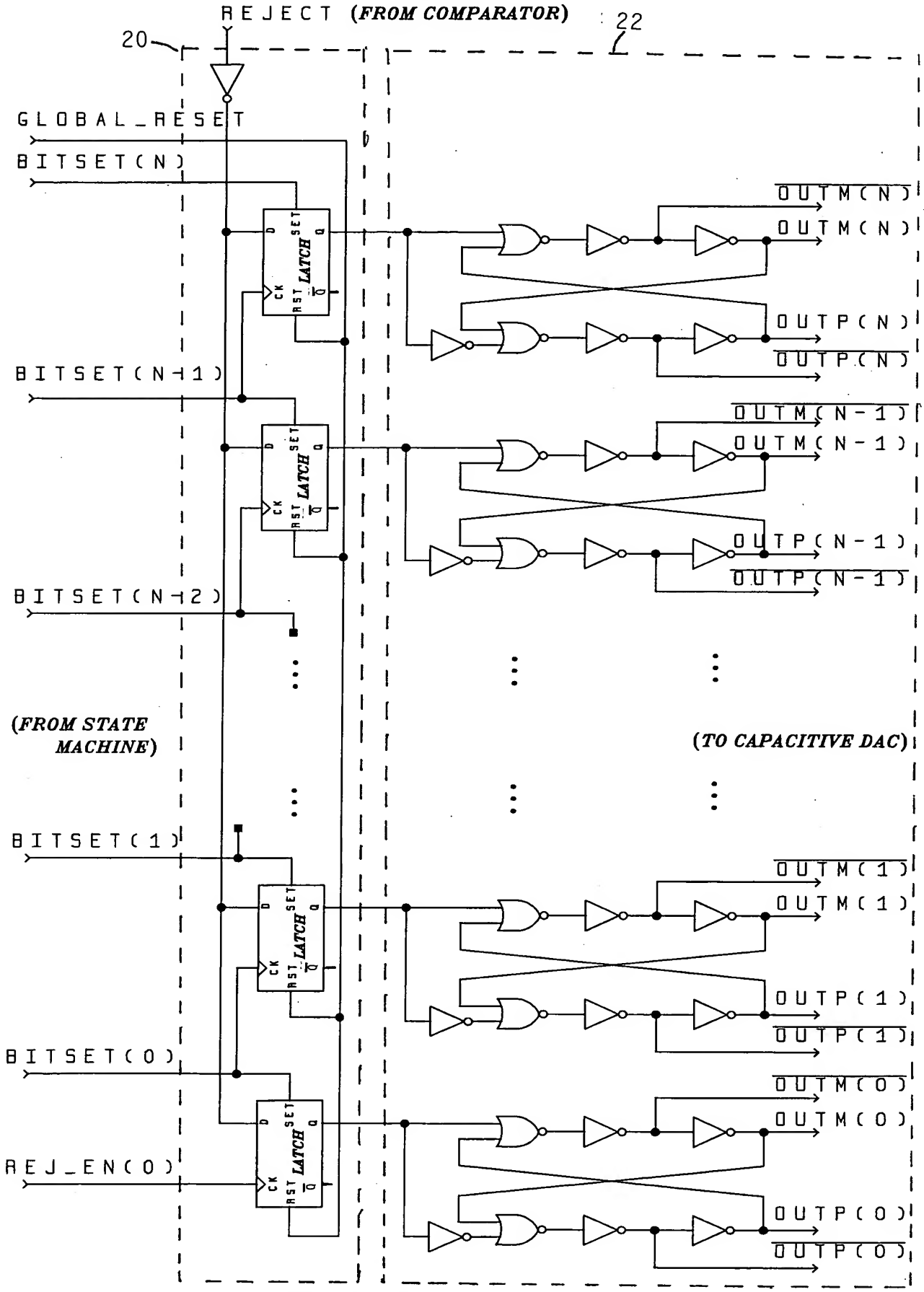

FIG. 2 (Prior Art)

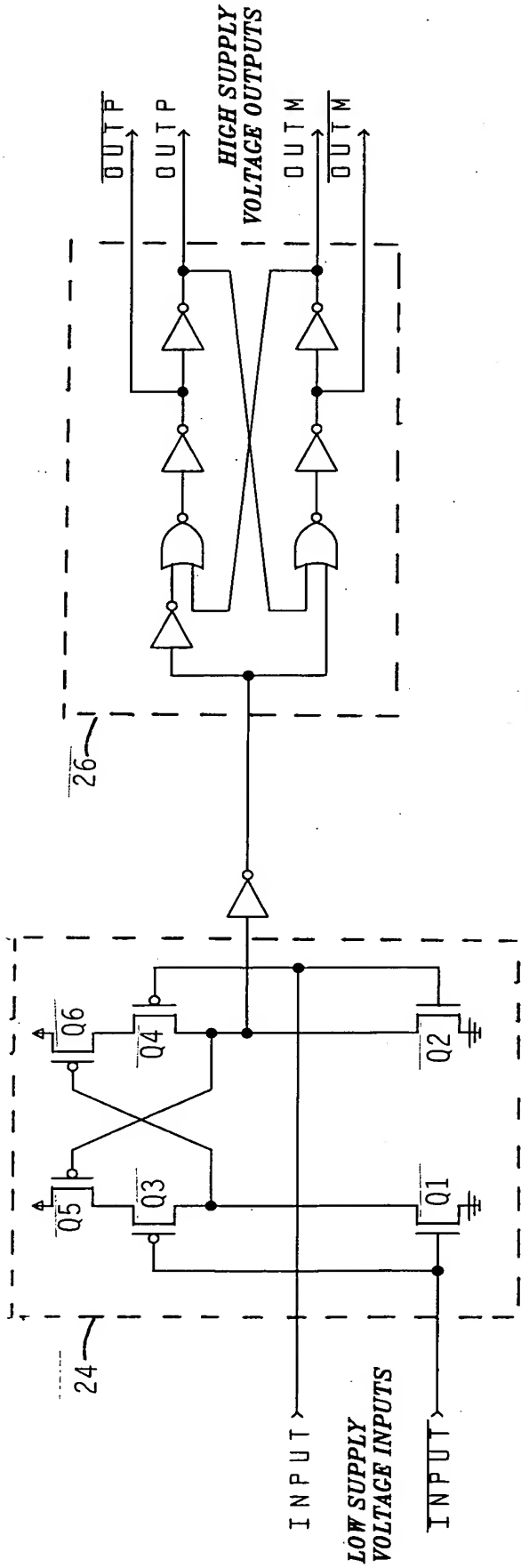

FIG. 3 (Prior Art)

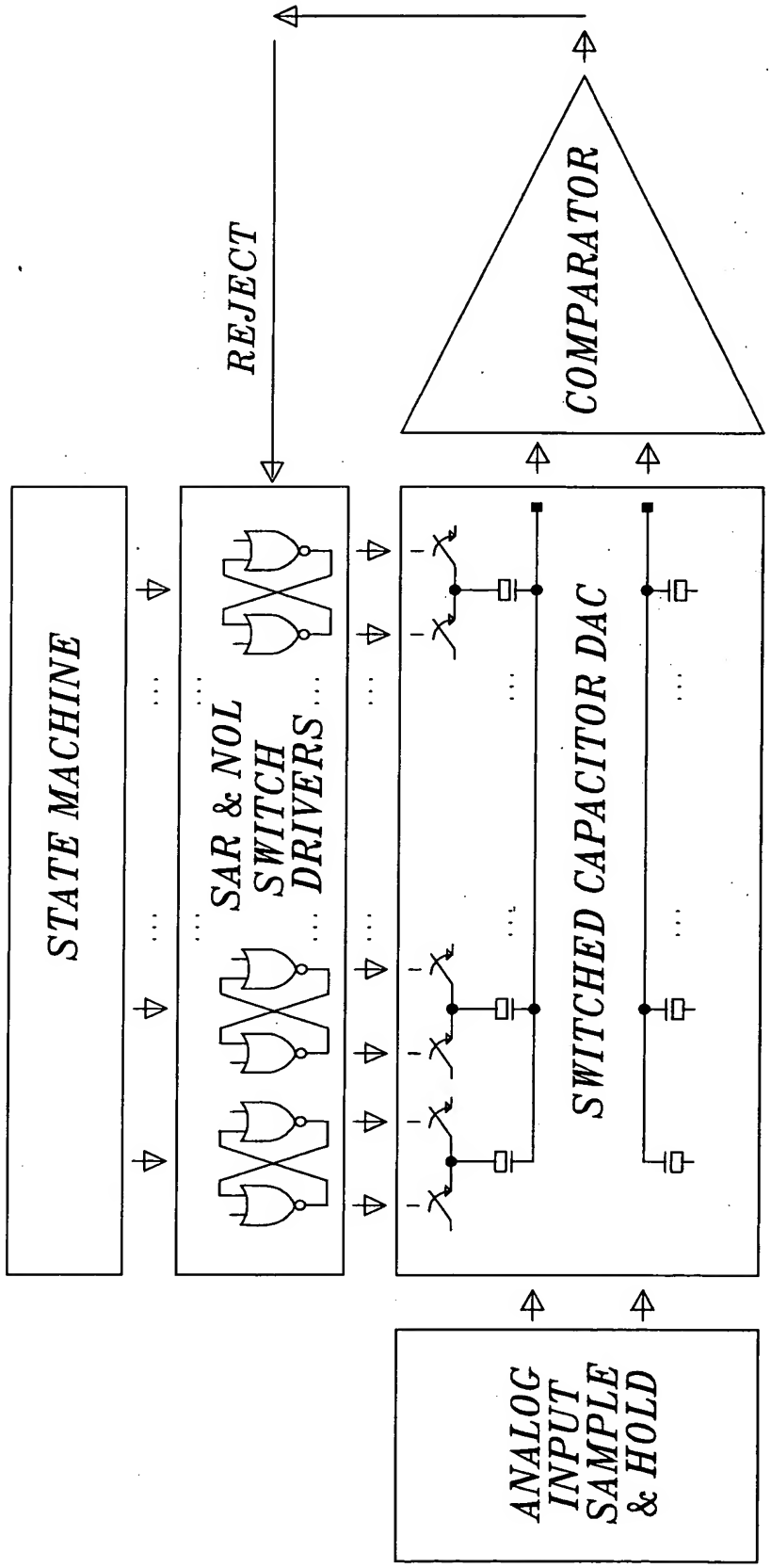
REJECT
COMPARATOR
STATE MACHINE
SAR & NOL SWITCH DRIVERS
SWITCHED CAPACITOR DAC
ANALOG INPUT SAMPLE & HOLD

FIG. 4

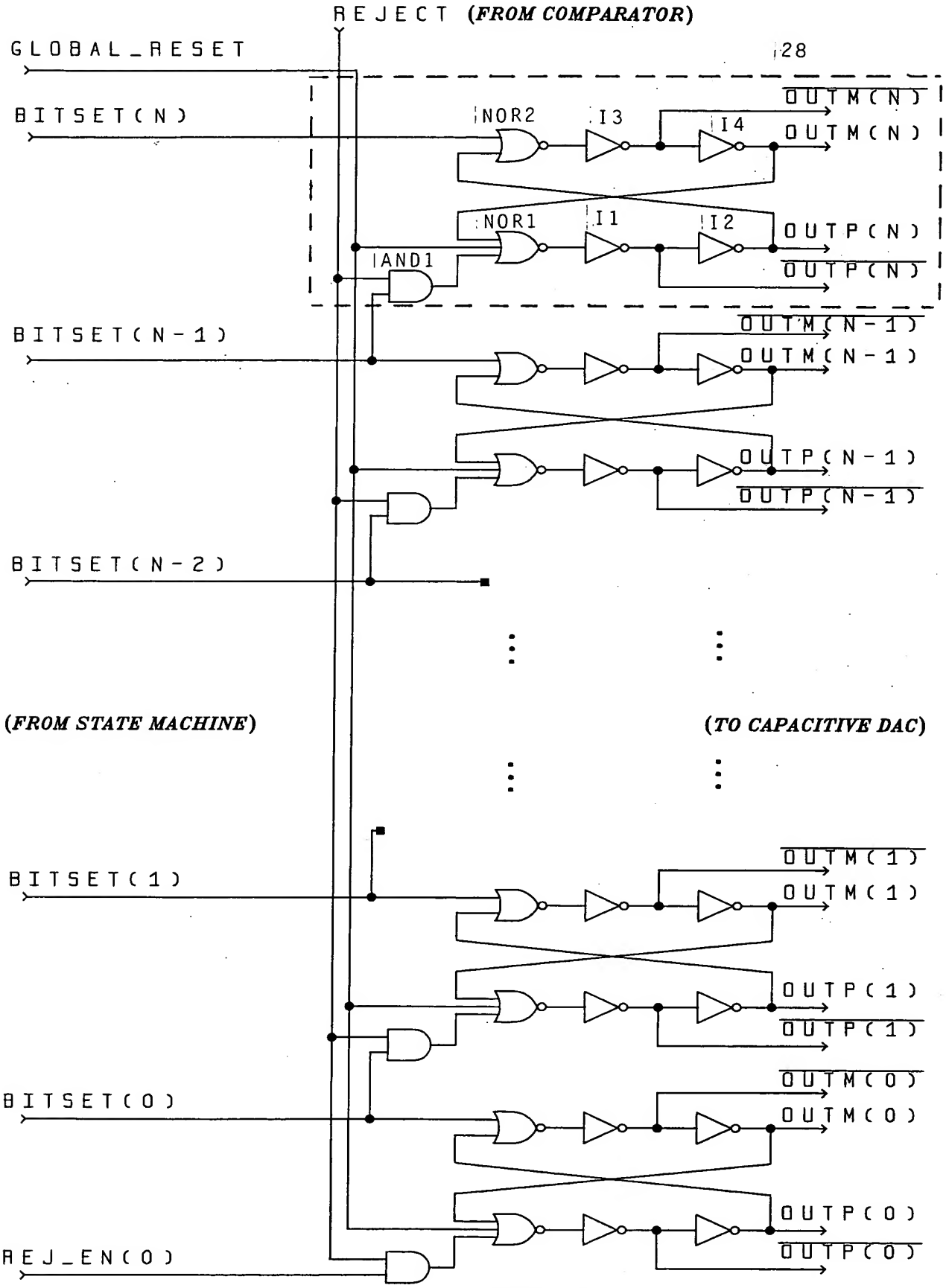
REJECT (FROM COMPARATOR)
GLOBAL_RESET
28
BITSET(N)
NOR2
I3
I4
OUTM(N)
OUTM(N)
NOR1
I1
I2
OUTP(N)
OUTP(N)
AND1
BITSET(N-1)
OUTM(N-1)
OUTM(N-1)
OUTP(N-1)
OUTP(N-1)
BITSET(N-2)
(FROM STATE MACHINE)
(TO CAPACITIVE DAC)
BITSET(1)
OUTM(1)
OUTM(1)
OUTP(1)
OUTP(1)
BITSET(0)
OUTM(0)
OUTM(0)
OUTP(0)
OUTP(0)
REJ_EN(0)

FIG. 5

NOR BASED SET–RESET LATCH

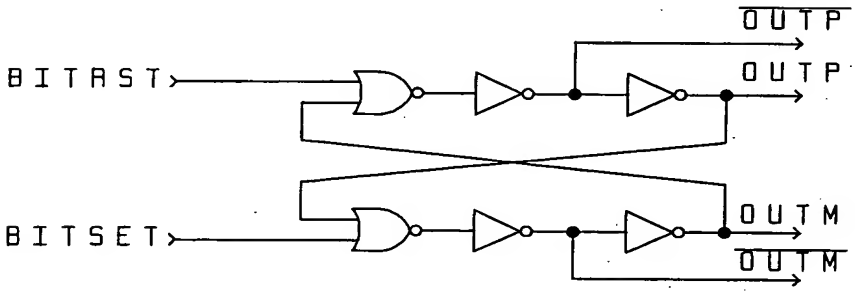

FIG. 6a

NAND BASED SET–RESET LATCH

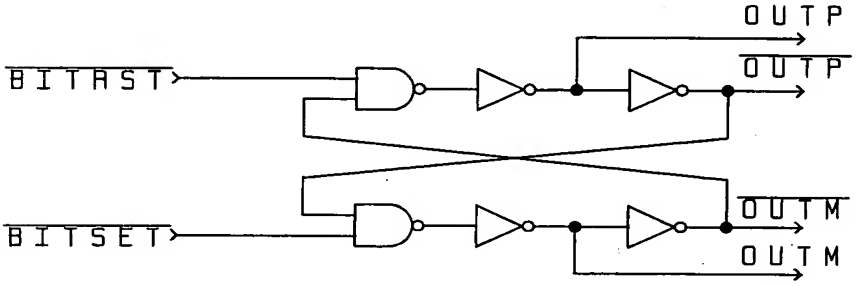

FIG. 6b

NAND BASED SET–RESET LATCH WITH SET & RST ENABLES

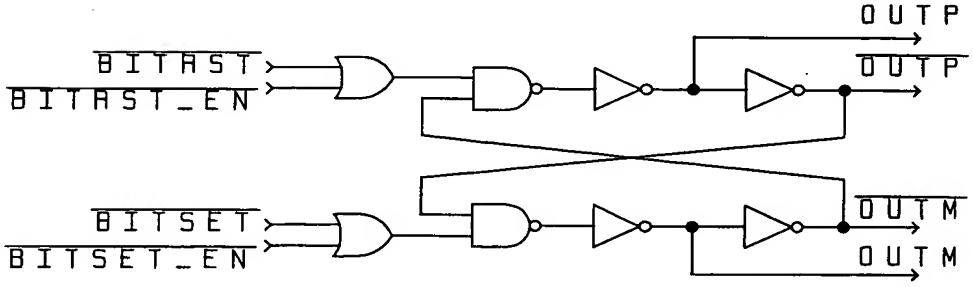

FIG. 6c

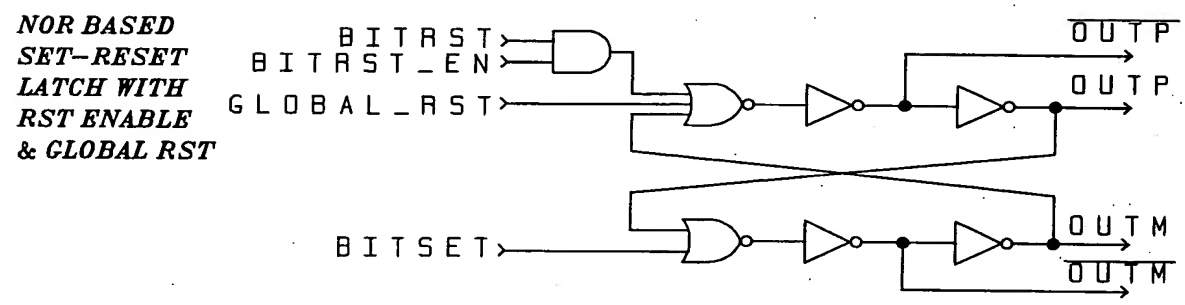

FIG. 6d

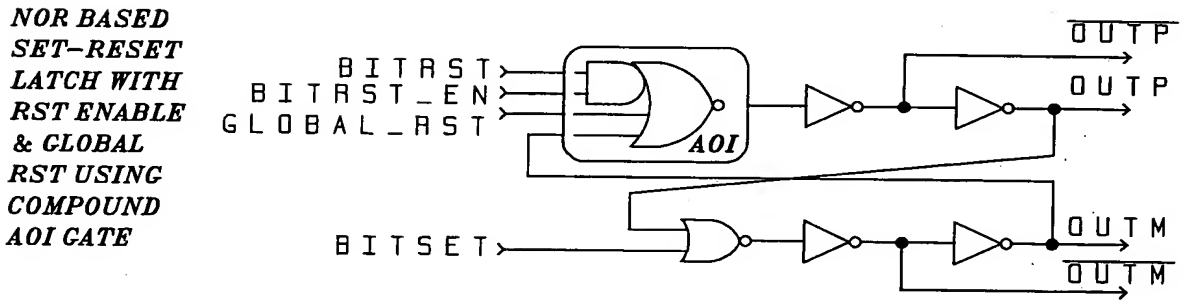

FIG. 6e

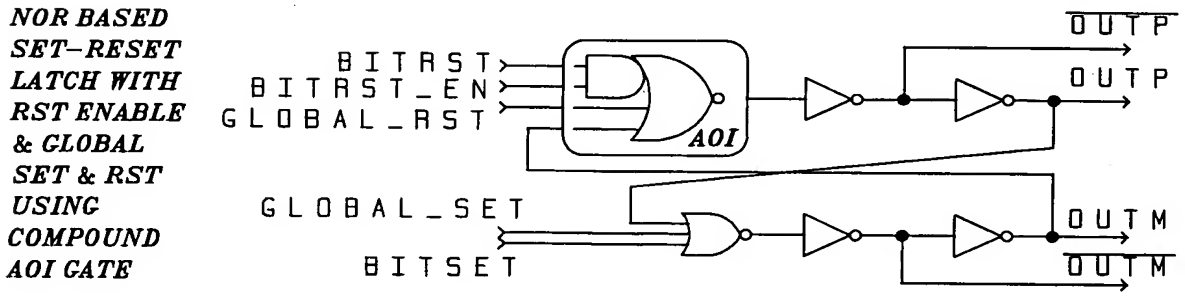

FIG. 6f

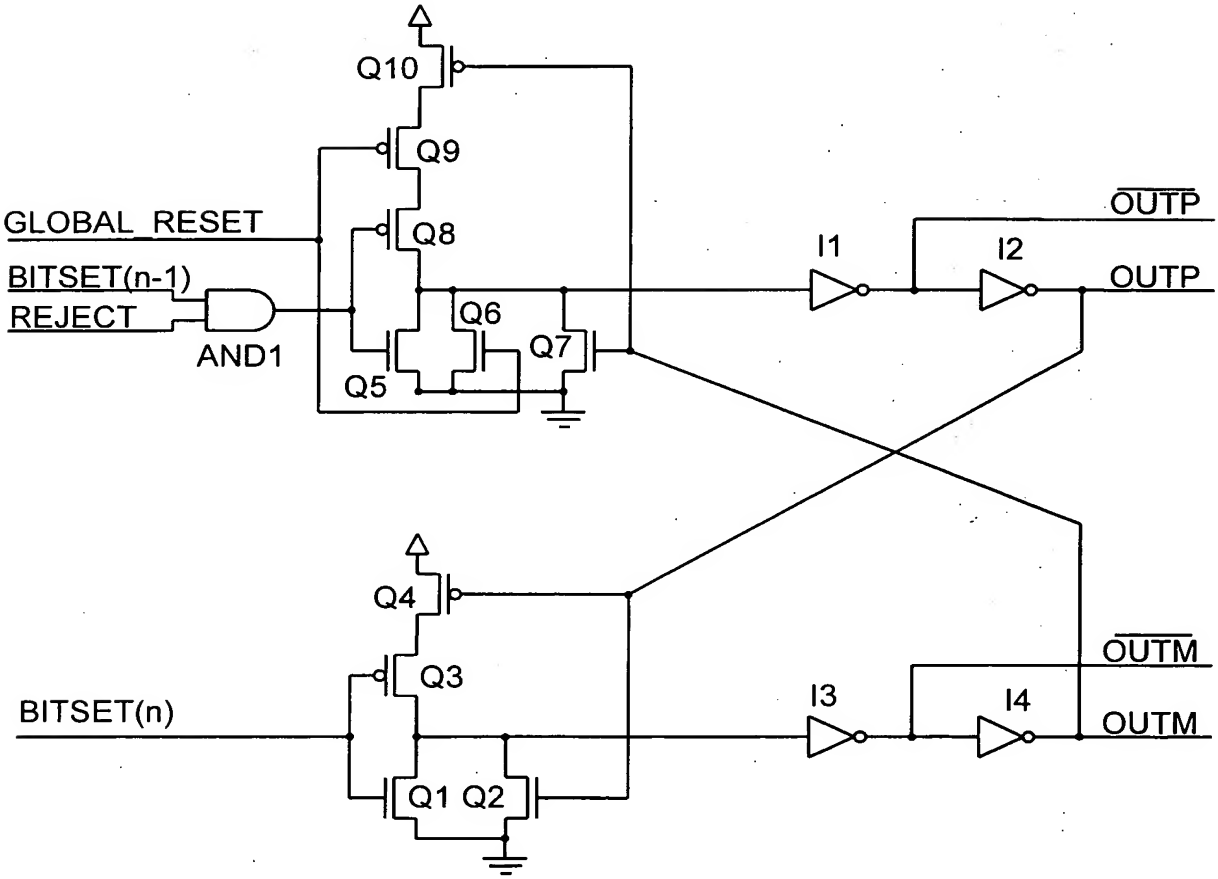
Q10
Q9
GLOBAL_RESET
Q8
BITSET(n-1)
REJECT
AND1
Q6
Q7
Q5
I1
I2
OUTP
OUTP
Q4
Q3
BITSET(n)
Q1 Q2
I3
I4
OUTM
OUTM

FIG. 7

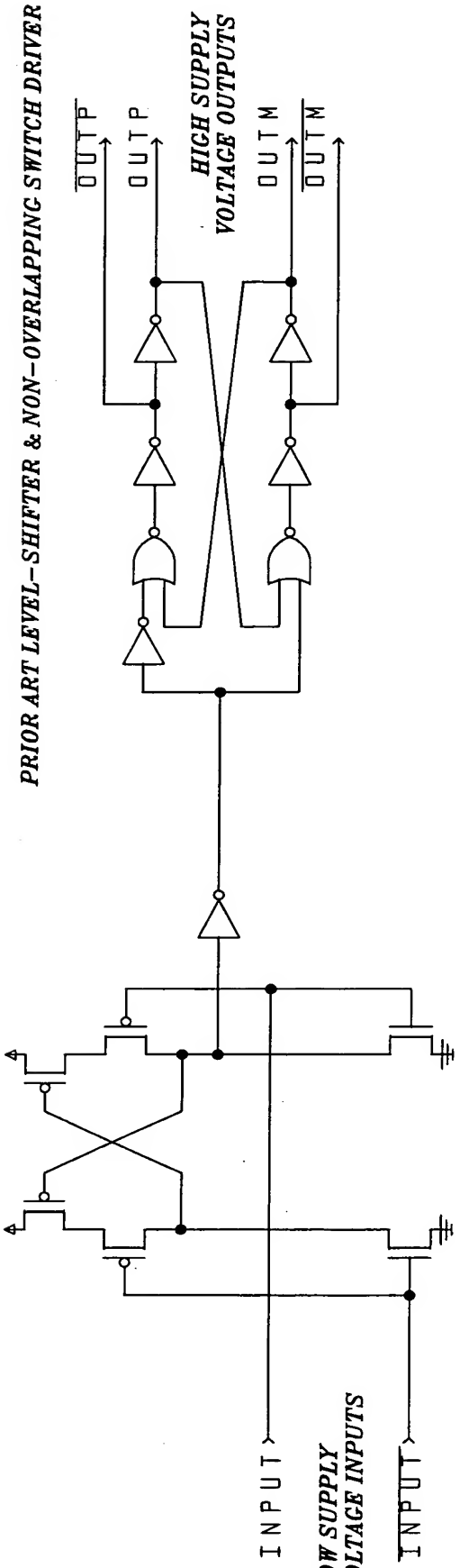
PRIOR ART LEVEL-SHIFTER & NON-OVERLAPPING SWITCH DRIVER
HIGH SUPPLY VOLTAGE OUTPUTS
OUTP
OUTP
OUTM
OUTM
INPUT
INPUT
LOW SUPPLY VOLTAGE INPUTS

FIG. 8

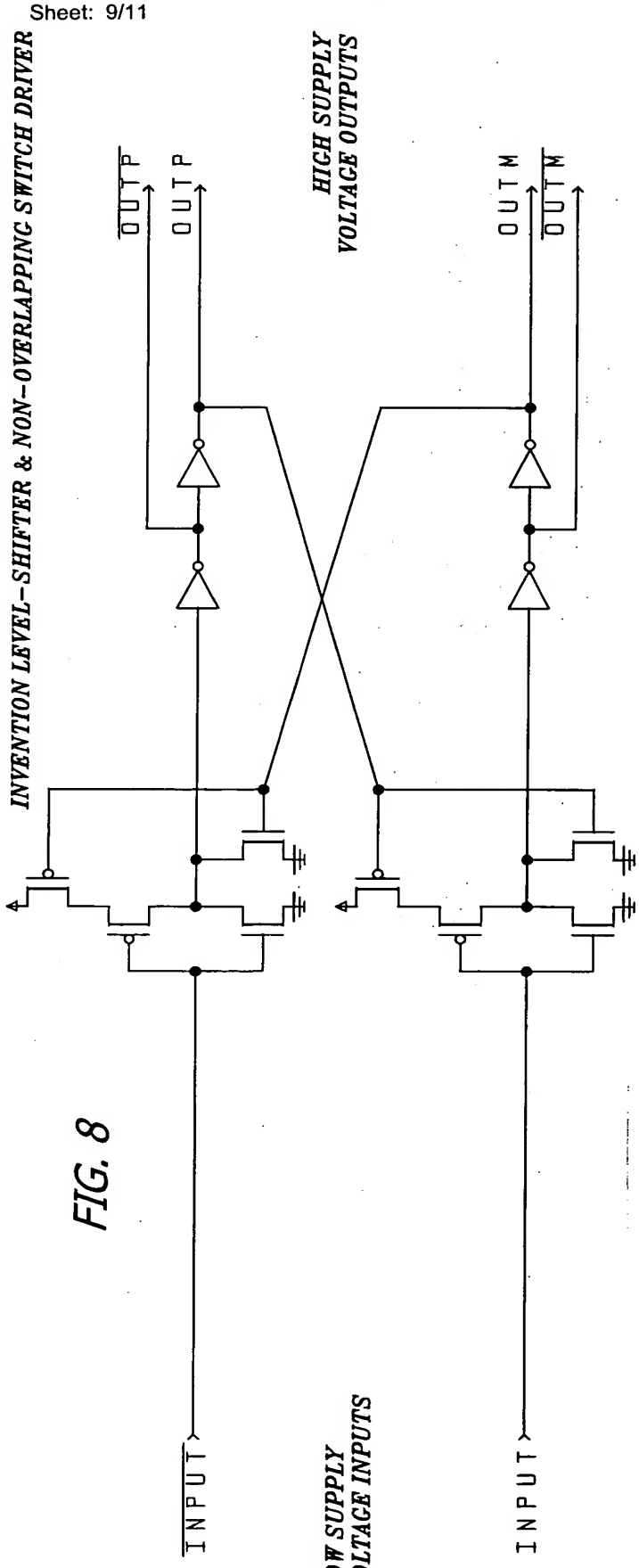
INVENTION LEVEL-SHIFTER & NON-OVERLAPPING SWITCH DRIVER
HIGH SUPPLY VOLTAGE OUTPUTS
OUTP
OUTP
OUTM
OUTM
INPUT
INPUT
LOW SUPPLY VOLTAGE INPUTS

FIG. 9

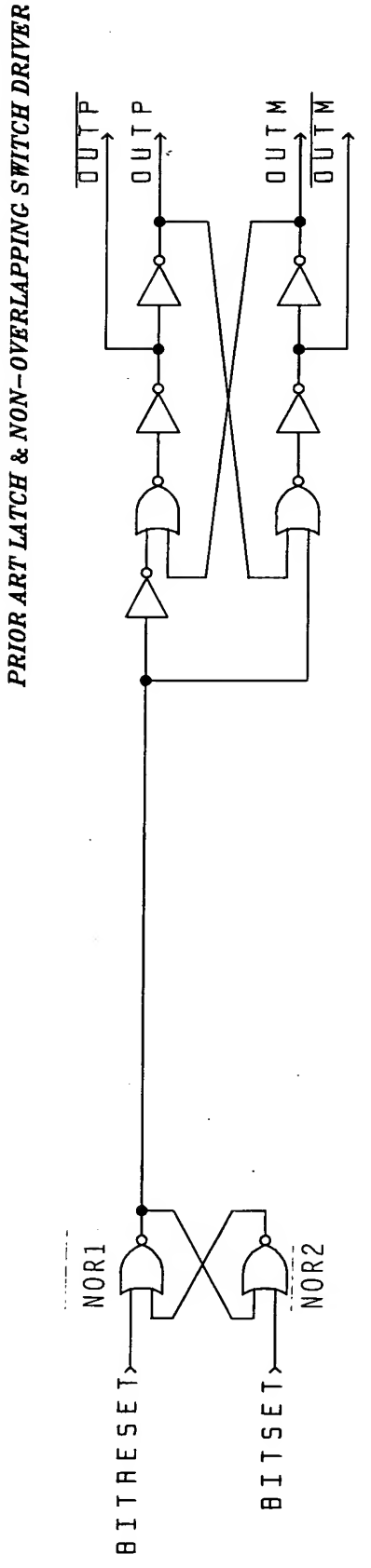
PRIOR ART LATCH & NON-OVERLAPPING SWITCH DRIVER
OUTP
OUTP
OUTM
OUTM
NOR1
NOR2
BITRESET
BITSET

FIG. 10

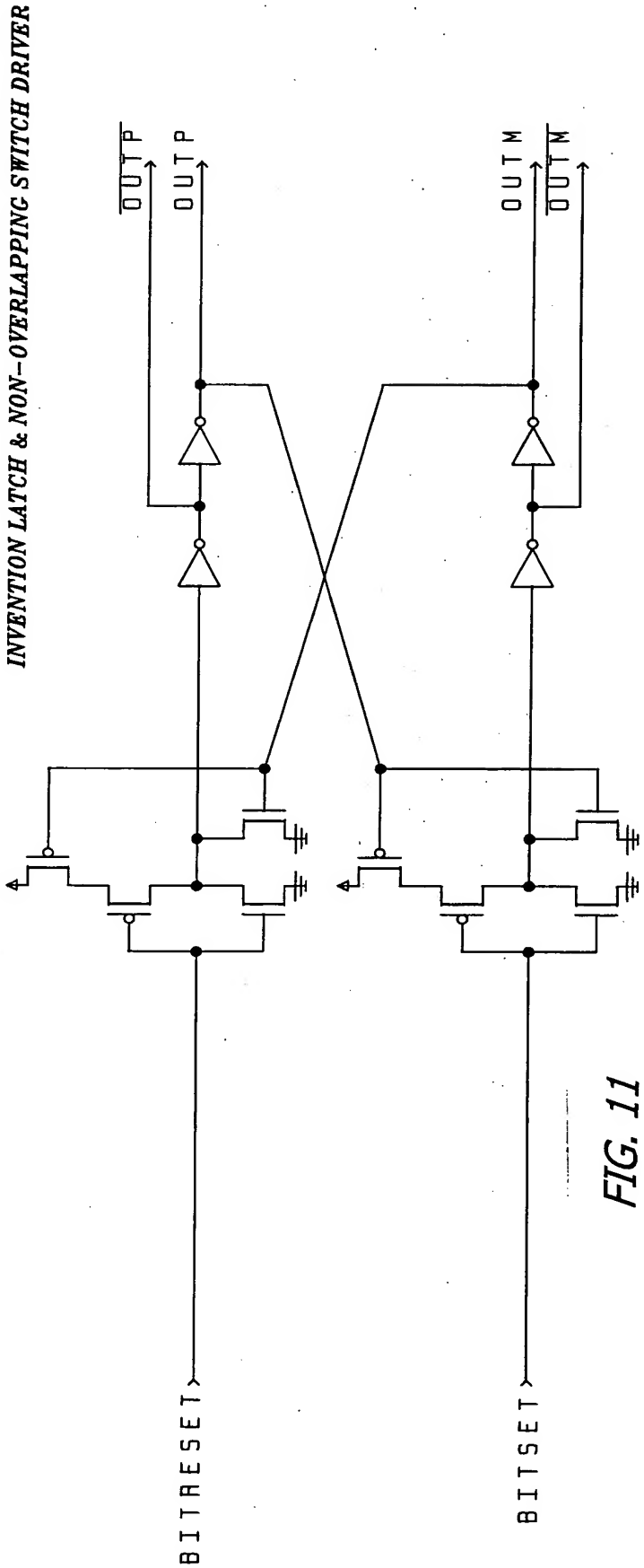
INVENTION LATCH & NON-OVERLAPPING SWITCH DRIVER
OUTP
OUTP
OUTM
OUTM
BITRESET
BITSET

FIG. 11

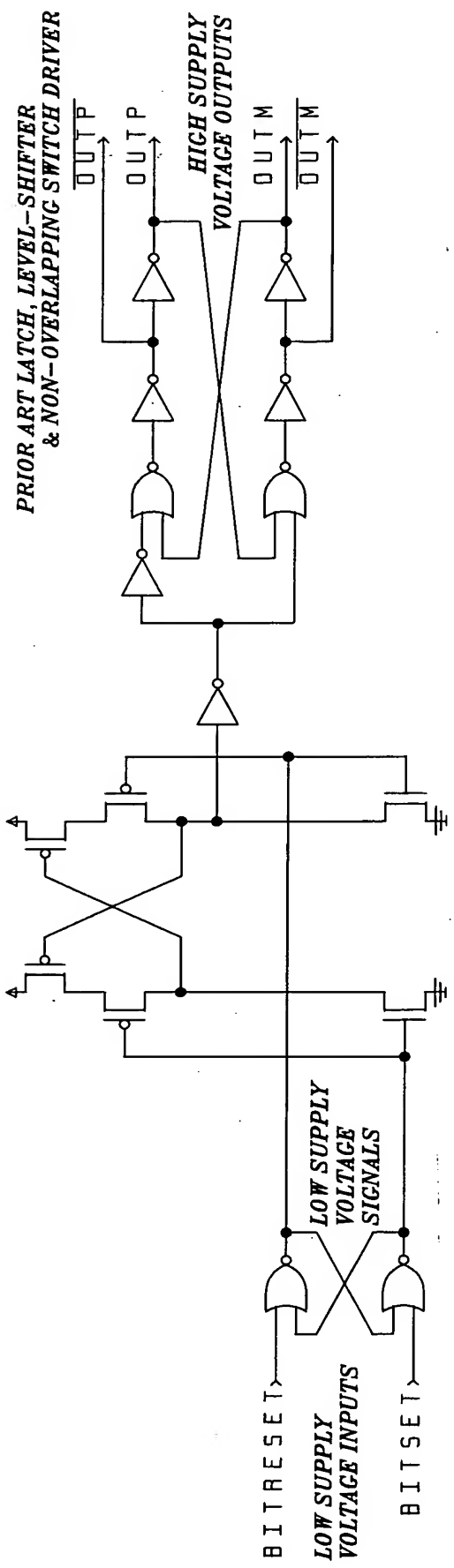
PRIOR ART LATCH, LEVEL-SHIFTER
& NON-OVERLAPPING SWITCH DRIVER
OUTP
OUTP
HIGH SUPPLY
VOLTAGE OUTPUTS
OUTM
OUTM
LOW SUPPLY
VOLTAGE
SIGNALS
BITRESET
LOW SUPPLY
VOLTAGE INPUTS
BITSET

FIG. 12

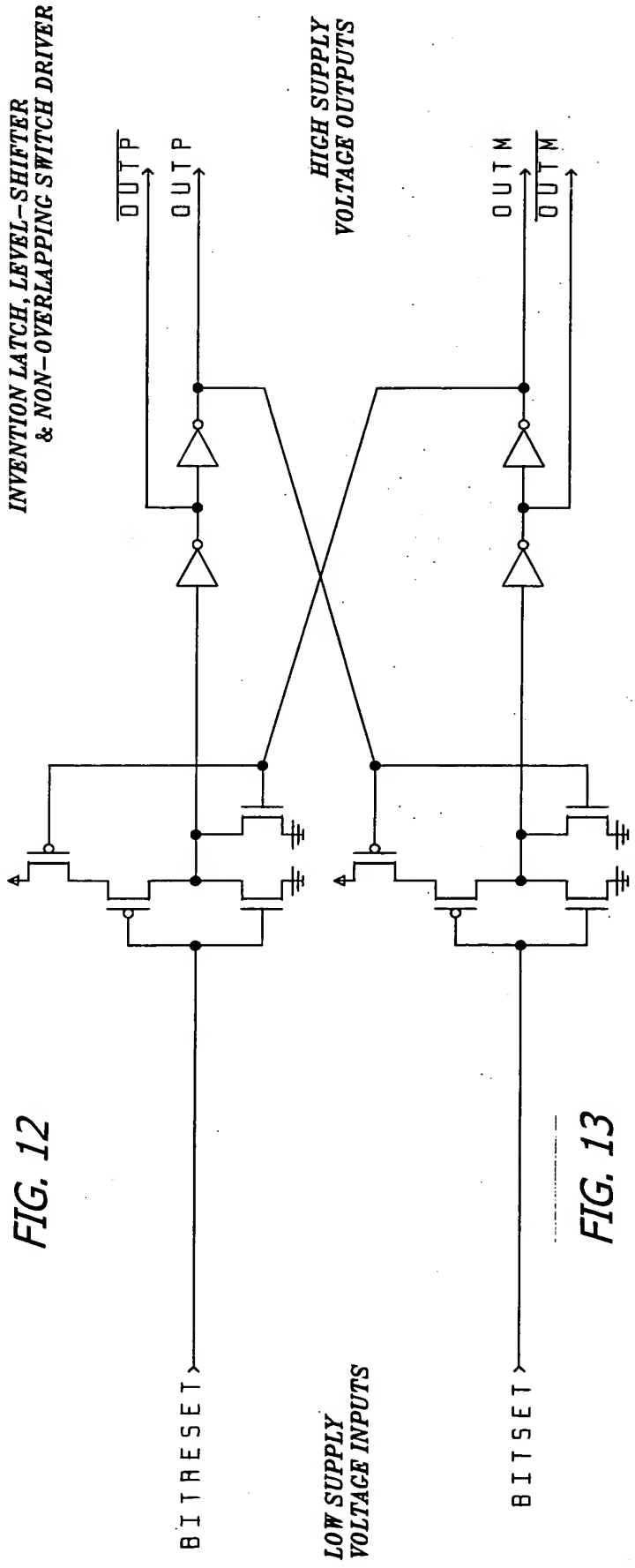
INVENTION LATCH, LEVEL-SHIFTER
& NON-OVERLAPPING SWITCH DRIVER
OUTP
OUTP
HIGH SUPPLY
VOLTAGE OUTPUTS
OUTM
OUTM
BITRESET
LOW SUPPLY
VOLTAGE INPUTS
BITSET

FIG. 13